REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated November 19, 2002 have been carefully reviewed by the Applicants. Claims 16-20 and 6-9 are currently pending, with Claims 16-18, and 20 being rejected. Claim 19 is objected to. Claims 16 and 19 have been amended. New Claims 21-35 have been added

Claim 16 is currently rejected under 35 U.S.C. 102(b) as being anticipated by Kim (JP 8-274198). In response, Claim 16 has been amended to patentably distinguish the present claimed invention from Kim. Specifically, Claim 16 has been amended to include forming an oxide layer on the surface of the semiconductor substrate, and forming a nitride layer on top of the oxide layer. The two layers are related to the planarization process as disclosed at page 9, lines 11-17 of the specification, and are not anticipated by Kim, or the combination of Kim and Lin, as described below.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lin (US 5960284). The Applicants respectfully traverse the rejection on the grounds that Lin does not teach each and every aspect of the invention as claimed. The rejection holds that:

> Lin (see e.g., figs. 7B and 8B), on the other hand, shows a step of forming a trenched gate-electrode comprising the step of planarizing the layer of polysilicon to a substantially planar orientation with a top surface of the semiconductor substrate.

Lin does not teach planarization of the polysilicon, but in fact teaches selectively etching back the polysilicon layer, as taught with respect to figures 7B and 8B, at column 5, lines 1-6. The selective etching of the polysilicon leaves the oxide intact. Planarization (e.g., through CMP) is not a selective process, in that a planar surface is produced by removing material at high points on the substrate, regardless of the composition. In figures 7B and 8B, the oxide clearly protrudes above the substrate surface. In view of the explicit teaching of selective etching of the polysilicon, Kim cannot be held to teach planarization.

In planarization processes, different materials may have different individual rates of removal, but a planar surface results when a surface is a composite having two materials with individually different material removal rates. The use of a nitride layer as an "etch stop" serves to slow down the material removal rate so that dimensional accuracy normal to the substrate is improved. In planarizing the polysilicon in the presence of the nitride layer, both polysilicon and nitride are removed in equal volumes and the process is not selective, but it is slowed by the presence of the nitride. Reducing the material removal rate is particularly desirable for shallow trenches.

Claim 16 has been amended to include forming an oxide layer on the surface of the semiconductor substrate, and forming a nitride layer on top of the oxide layer. The two layers are related to the planarization process as disclosed at page 9, lines 11-17 of the specification, and are neither taught nor suggested by the combination of Kim and

Lin. Thus, Claim 16 and dependent Claims 17, 18, and 20-27 are patentably distinguished from the combination of Kim and Lin.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lin (US 5960284) and Jaeger. The Applicants respectfully traverse the rejection on the grounds that combination of Kim and Lin does not teach or suggest each and every element of Claim 18 as described above, and Jaeger does not remedy the defect of Kim and Lin.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lin (US 5960284) and Jaeger, further in view of Wolf (US 3873371). The Applicants respectfully traverse the rejection on the grounds that combination of Kim and Lin does not teach or suggest each and every element of Claim 20 as described above, and Jaeger and Wolf do not remedy the defect of Kim and Lin.

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Claim 19 has been amended to include all of the limitations of base Claim 16. Applicants submit that Claim 19 is now in condition for allowance, having been amended in accordance with the Examiner's requirements for allowance. The Applicants further submit that new Claims 28-35, being dependent upon amended Claim 19, are also in condition for allowance.

In summary, the Applicants assert that Claims 16-35 are in condition for allowance, and earnestly solicit such action by the Examiner.

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Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claim 16 has been amended as follows:

16. A method for fabricating a semiconductor device with a trenched gate comprising:

forming an oxide layer on the surface of a semiconductor substrate;

forming a nitride layer on said oxide layer;

etching a trench having substantially upright vertical sidewalls and a bottom surface in said semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

Claim 19 has been amended as follows:

19. [The method of claim 16]A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode;

forming a control gate electrode on a top surface of the inter-gate dielectric layer, and

wherein the step of forming a source region and a drain region comprises a self-limiting diffusion process.